

# Standard High-Reliability Integrated Circuit Logic Packaging

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*A family of standard, high-reliability hardware used for packaging digital integrated circuits is described. The design transition from early prototypes to production hardware is covered and future plans are discussed. This article includes detail descriptions of the interconnection techniques, connectors and related hardware available, both at the microcircuit packaging and main-frame level; general applications information is also provided.*

## I. Introduction

Standardized modular hardware for the packaging of integrated circuit (IC) logic systems was described in Ref. 1, when development was in the early prototype stage. Since that time, a considerable quantity of hardware has been produced and installed in the DSN stations. This article will review the design transition from early prototypes to production hardware, deal with the production phase, and discuss some user application considerations, and future plans.

The modular packaging hardware, as reported in Ref. 1, evolved at two distinct levels. The first level is a plugable subchassis (Figs. 1 and 2), which packages and interconnects up to 144 ICs of the 14- or 16-pin dual-in-line package (DIP) type. This subchassis was designed to serve (by replacement at the subchassis level) as the first line of maintenance in the DSN stations, for the logic packaged therein. Approximately

1400 of these subchassis have been manufactured to date. Cost data are provided in Table 1. Interconnection of the ICs, which plug into special high-reliability (hi-rel) sockets, is by wirewrap, which can be accomplished on a fully automatic machine. The second packaging level is that of the main chassis, which provides the mating receptacles and interconnections for the several subchassis (usually but not necessarily more than one) required to implement a functional unit. Whereas the one subchassis design has been utilized as a standard for all applications, the main chassis design has been fully standardized only at the level of the subchassis mating receptacle (Fig. 3), because of variations in the number of subchassis per subsystem, presence of other digital hardware and display devices, the system of subsystem partitioning (i.e., breakdown into independent drawers, perhaps each with its own power supply), all related to the need for accessibility for testing, and the number of wires (cables) to be carried into the chassis.

This report will also describe three main chassis designs which have been used to package a majority of the subsystems implemented to date and will list the documentation available to the potential user.

## II. Detail Description

Figure 2 shows the subchassis design adopted. Subchassis may carry part numbers 9457999-1 or -2 (the first lot of 175, now obsolete, carried part number 9457085-1). The -1 and -2 suffixes cover minor differences in manufacturing; all subchassis, including obsolete model 9457085-1, are fully interchangeable to the user. The subchassis holds 144 of the 14- or 16-pin plugable DIP ICs. A half-size subchassis has been documented but has not been fabricated to date.

The design is based on an aluminum base plate which serves as the ground plane. A power plane is laminated over the base plate, on the wirewrap side (Fig. 4). This arrangement provides excellent ground-plane and power distribution characteristics, suitable for 54S (Schottky-clamped) ICs. Plane noise is insignificant when compared with the noise margins of 54-series circuits (about 1 volt). Ground and power connections to the IC sockets are made by wirewrapped connections on posts press-fitted into the ground and power plane (see Fig. 5). The standard subchassis comes with one ground and one power post pre-installed at locations convenient to the power and ground pins of 14- and 16-pin ICs. Users of larger, high-speed LSI packages may install additional ground and power pins in spare holes provided for this purpose, if required to minimize lead length (ground and power connections should not exceed 1 in. (2.54 cm) for any 54-series circuit).

Strip sockets (Fig. 6) permit the use of LSI modules or any module whose pins are disciplined to multiples of 0.1-in. (2.54-mm) centers. Sockets are press-fitted into the base plate (ground plane). The tuning fork contact provides sufficient tension for a reliable contact, and, when formed from beryllium-copper alloy and heat-treated, is capable of expanding to accept larger diameter pins, and after withdrawal of these pins, recovering to grip the very thin pins used on many ICs. Broken contacts may be replaced individually.

The subchassis interface connector provides 204 pins, consisting of sixty-eight 3-pin modular connectors. These 3-pin connectors, shown in Fig. 7, are individually replaceable. Four additional 3-pin connectors, providing for ground connections, are made with tin-plated brass bodies.

The subchassis is mounted on the mating receptacle (in Fig. 3, both wirewrapable and wire-crimp terminations are shown) with two jack screws. In the interest of providing for maximum flexibility in overall chassis design (which varies

widely according to system requirements), these jack screws are the sole method of subchassis mounting. This arrangement has been drop-tested to confirm handling and shipping survival.

Jack screws are assembled internal to the subchassis as shown in Fig. 8. The first lot of 175 subchassis did not use the lubricated thrust washer and had difficulty with galling of the jackshaft on the housing. As a result of this galling, and a tendency for personnel to apply more torque than necessary to fully seat the jack screw, roll pins were sheared off. The present model subchassis (9457999-1 or -2) uses a larger diameter roll pin, and replacement parts of the newer design are available for the older subchassis.

The mating receptacle uses tuning fork contacts housed in insulating sleeves (aluminum sleeves for grounded contacts), which are press-fitted into holes drilled in the aluminum base plate. Contacts are individually replaceable and are rated at 5 amperes. The receptacles shown in Fig. 3 are available with either wirewrap terminations (which may also be soldered) or wire-crimp terminations.

## III. Development Progress

The present design differs from the one pictured in Ref. 1 in the following details. The first prototype used an extruded aluminum section (Fig. 9) as the basic structure. Note that the new design (Fig. 2) uses a flat plate with attaching rails which serve to stiffen the plate and protect the wrap-posts from damage. Experience at the JPL machine shop indicated that the aluminum extrusion used in the original design would reduce costs by eliminating the machining costs of the separate rails. This experience was not sustained when commercial bids were received. The extrusion apparently raised fears of possible production difficulties and all bids contained a substantial hedge against these difficulties. Low bids were (for 200 parts) \$200 for machining the extrusions, and \$112 for machining the flat plate. The four rails and one connector retainer bar cost \$25, for a total of \$137 for the assembly. Other considerations include the cost of the raw extrusion which balances out with the cost of labor and screws required to assemble the rails. A decision was made to use the flat plate and separate rails.

Because of schedule commitments and because the modular connectors (Fig. 7) were the longest lead-time component, a cost plus incentive fee contract was let for these connectors prior to completing a thorough worst-case analysis of the connector mating; a problem area was noted when this analysis was performed. Referring to Fig. 10, note that the blades of the modular connector are recessed into a channel for protection during handling. The nylon sleeves (which form the

mating receptacle) must fit into this recess. In addition to protecting the blades, the initial contact between the subchassis channel and the receptacle sleeves serves to guide the subchassis connector blades into the receptacle "tuning fork" contacts as the jack screws are engaged. This feature is a desirable addition to the pair of guide pins which are also used for alignment, because the jack screws, used to apply the 200 pounds (890 newtons) of force required to mate 216 connector blades, deprive the operator of any feeling for misaligned, i.e., jammed blades. For this reason, the width of the subchassis recess was designed to barely accommodate the mating nylon sleeves. However, worst-case analysis showed that insufficient tolerance had been allowed for the small random mislocations of the nylon sleeves. It was then found necessary to increase the spacing by 0.005 in. (0.127 mm). Since it was undesirable to increase the height of the connector bodies due to the incentive fee contract, it was decided that 0.005 in. (0.127 mm) would be milled off the base plate, as shown in Fig. 10. When a contract was let for a second manufacturing source and second set of tooling, this milling operation was deleted and the connector height increased. The new connectors use a different body color.

The original prototype and the first 175 production subchassis also used power and ground pins with threaded sleeves, held in place with a No. 1 hex nut (Fig. 8 of Ref. 1), whereas present production uses a press-fit sleeve. These early subchassis carry part number 9457085-1. Subchassis using pins with press-fit sleeves (1188 have been manufactured to date) carry part numbers 9457999-1 or -2. The -1 suffix applies to subchassis manufactured by Masterite Industries, while the -2 suffix applies to Fabri-Tek production. They are fully interchangeable to the user. The original decision to use pins with threaded sleeves was based on ease of repair. The press-fit sleeves require special tooling to remove and replace, particularly after the subchassis has been wirewrapped. However, the pins with threaded sleeves and nuts presented the following problems:

- (1) They were relatively costly, both in per item cost and installation labor. The savings using press-fit sleeves is \$60 to \$70 per subchassis, or 10 to 15 percent of the subchassis cost.
- (2) They were sole-sourced.
- (3) Quality control of the threads proved difficult, and some pins failed to tighten down properly. Inspection was difficult.

The strip sockets (Fig. 6) are derived from the Standard Hardware Program of the Naval Avionics Facility, Indianapolis.

As used in the Navy program, these sockets mated with the 0.020-in. (0.5-mm) thick blades of a circuit board (IC flat packages were mounted on the circuit board). The tuning fork style of contact, using beryllium-copper alloy, was selected because it had the potential for accommodating the wide variety of pin sizes used on the various ICs and other commercial DIP circuit modules without damage, providing exceptionally good contact retention for all packages. However, to accommodate the 0.010-in. (0.25-mm) thick blades of the typical DIP packages, it was necessary to have the manufacturing tooling redesigned to provide an 0.006-in. (0.15-mm) maximum contact opening. In Ref. 1, it was stated that these sockets were commercially available. However, the material used by that vendor was phosphor-bronze alloy, a material which exhibits aging fatigue, and negotiations to substitute beryllium-copper alloy were never successfully completed. However, two other sources of the Navy contact (which used beryllium-copper alloy) were willing to re-tool as required to provide the JPL-specified contact opening.

## IV. Documentation and Manufacturing

All component parts (including those used on the subchassis mating receptacles) are covered by JPL detail drawings or, in the case of commercial components, either by JPL specification control drawings or military/federal specifications.

Subchassis have been manufactured for JPL by two different companies. The first lot was built at a unit cost of \$836 by Masterite Industries (the only bidder): a total of 429 subchassis were manufactured. The second source, the National Connector Division of Fabri-Tek, Inc., has produced 943 subchassis at an approximate cost of \$550 each. The price reduction is thought to be due to:

- (1) The additional competition available as evidence of JPL's intent to purchase significant quantities became available.
- (2) Improved tooling design, more automation and better production controls used by the second source.

With the exception of the off-the-shelf commercial components, JPL owns the production tooling manufactured by both of the above companies. Two sets of tooling exist because the production contracts overlapped, and because of our desire to obtain two sources. The tooling produced by Masterite is now in storage in a federal warehouse, while the tooling produced by Fabri-Tek is now at that company or its subcontractors. The Fabri-Tek tooling represents an investment of approximately \$55,000, or about \$58 per subchassis produced to date (10 percent of the per unit price).

Major items of tooling include punch-press dies for the contacts of the modular connector and the IC strip socket, and injection molds for the connector bodies. There is also a punch-press die for the power plane, and drill jigs for the mounting rails. There are also fixtures which assist in the loading of contacts and wrap-posts, and which otherwise aid in assembly.

## V. Quality Control

Contractor quality control is governed by JPL Specification ES509281, "Quality Control Requirements for Subchassis, IC Logic Packaging, Detail Specification for." This specification includes all applicable portions of GMO-50139-GEN, The General Specification of Quality Control Requirements for Operational Support Equipment, plus additional material specifically applicable to subchassis. Additional detail specifications have been written to cover the IC sockets and modular connectors. Workmanship is inspected to QAWS 200.60, a Quality Assurance Workmanship Standard written specifically for the subchassis. It has proven necessary to have a JPL inspector present at the contractor's facility for first article inspections at the component level, and for the final inspection of each subchassis. In this way, any necessary rework can be accomplished with assurance that it is properly performed. It has also proven highly desirable to utilize the same inspector for each successive production lot, because there is very substantial learning function. The location of defects or omissions among the thousands of contacts and wrap-posts (any one of which is costly to the ultimate user) requires several days of on-the-job training, during which time the new inspector learns from his oversights.

## VI. Procurement Lead Times

Procurement lead times vary significantly according to the situation encountered when competitive bids are solicited. If the tooling is utilized by a past manufacturer, finished subchassis will be available 12 to 14 weeks after receipt of order. An additional 10 to 14 weeks should be allowed for procurement procedures required prior to placement of order. If the tooling is furnished to a vendor who has not utilized it before, an additional 4 to 12 weeks will be required for tooling adaptations, first article inspections, and production de-bugging.

Because of these lead times, a stock of about 100 to 250 subchassis is maintained. Delivery from stock is made on approval of the Section 338 manager. Table 1 lists the subchassis and accessory components available. Orders are not normally placed unless a requirement for at least 100 subchassis has been accumulated, to take advantage of the price break.

## VII. Subchassis Application Guidelines and Conventions

### A. Installing LSI Modules

The strip sockets permit the use of LSI modules having more than 16 pins. By installing additional strip sockets, as shown in Fig. 11, any pin row spacing based on integer multiples of 0.1 in. (2.5 mm) can be accommodated. Ground pins may be removed if necessary. Documentation should consist of a tabular list of the subchassis coordinates where strip sockets are to be added and ground pins removed (if any).

### B. Pin Numbering System

The subchassis is divided into four identical sections. Referring to Fig. 12, which shows one of these sections, note that each section has 18 (9 pairs on 0.3-in. (7.6-mm) centers) strip sockets, with 35 pins per row. Allowing for one unused pin between ICs (required for package end overhang), each pair of rows accommodates four 16-pin DIP modules. The numbering system is also shown in Fig. 12. Note that pins are numbered 101 through 135, with the second section numbered 201 through 235, etc. Utilizing this numbering system, pin No. 1 of 14- or 16-pin DIPs are installed at contacts 1Y101, 1Y110, 1Y119, and 1Y128; and for the second row at 2Y101, etc. ICs in the second section are installed at 2Y101, etc. This numbering system was devised with the expectation that significant numbers of larger LSI modules would be used. Their location would be designated per the location of their pin No. 1. However, some engineers whose applications have been limited to 14- and 16-pin ICs have thought the above system too cumbersome, and have designated socket positions using a conventional socket numbering system. A useful technique for troubleshooting on the wirewrap side consists of colored plastic sleeving installed on the unused pins between "sockets," specifically pins 9, 18, and 27 in each row of 35.

### C. Power Short Circuits

If a subchassis is found to have +5 volts shorted to ground, an instrument is available for locating the fault without removal of ICs or wirewrap: The IC Fault Locator Model CL-1 is manufactured by the Concept Electronics Corp.

### D. IC Installation and Removal

Because of the high contact retention force, IC pins may tend to crumple unless installed with the aid of an insertion tool which supports the pins and holds the dual pin rows in alignment, 0.300 in. (7.6 mm) on center. Figure 13 shows vector tool P157. Some difficulty may be experienced because the sides are not 0.310 in. (7.874 mm) apart, as required to align leads to 0.300-in. (7.6-mm) centers. The tool shown was

modified by replacing the tool's rivets with machine screws, after which the sides were bent as required to provide  $0.310 + 0.005 - 0.000$ -in. ( $7.87 + 0.127 - 0.000$  mm) separation. It is also very difficult to remove an IC without bending the leads unless they are pulled with the aid of a special IC puller. Figure 13 shows an Augat T114-1 puller.

### E. Power Supply Bypassing

The subchassis power plane is bypassed for high-frequencies with twenty-four 51,000 picofarad capacitors. However, the power supply leads may ring in the 100-kHz range in response to power loading which varies according to the logic states of the ICs, unless additional medium-frequency bypassing is used. Two 35-microfarad capacitors should be installed on the terminals provided on the front rail for this purpose, and connected to the nearest power plane power pin with short, direct leads. Other terminals are available for bypassing auxiliary power supplies. It may be necessary to install small low-inductance capacitors near the ICs which use these auxiliary supply voltages, in order to prevent noise spikes from coupling into other logic.

### F. Line Terminations

The subchassis provides an excellent ground plane effect, which is carried through the mating receptacle by four ground connectors. Twisted pairs may be terminated outside the subchassis, on the ground bus (see Fig. 3), if the connection inside the subchassis (to the driver or terminating resistor) is limited to about 6 in. (15 cm).

### G. Repair Tools and Maintenance Procedures

Figures 14 and 15 show the tool kits available for the repair and modification of subchassis and interface receptacles, including the replacement of broken pins and the installation of extra pins or sockets. Maintenance Procedure MP511469 governs the maintenance of subchassis, and MP511709 governs the maintenance of wirewrap interface receptacles.

### H. Additional Information for Engineers and Contractor Users

In many instances, detail logic design and layout of the logic on the subchassis is accomplished by JPL subcontractors. It is necessary to provide these contractors with some applications information and restrictions. TRD-338-954107-01 was written as the mechanism for including these application standards in a recent contract. In order to facilitate the inclusion of this material in all applicable contracts, it will be published as a released JPL document. This document covers the use of special tools for installing and extracting ICs, the necessity for short (1 in. (2.54 cm) maximum) ground and

power connectors to ICs, the permissible module pin sizes, power supply bypassing, the designation of JPL FS505770 as the specification covering wirewrapping and repair procedures.

## VIII. Chassis Design

The subchassis receptacle design uses contacts and nylon sleeves which are press-fitted into an aluminum plate. It is thus possible to design a single large plate which will serve as the receptacle for several subchassis, as shown in Fig. 3 of Ref. 1 and reproduced here as Fig. 16. This procedure is customary in commercial or military products with substantial production runs. However, the DSN usually does not require enough copies of one functional unit to justify the design cost of a custom plate (even after subtracting the cost differential between a modular receptacle system and the large plate). In addition, the DSN design requirements for standardized packaging hardware emphasize the advantages of the off-the-shelf components available at the highest reasonable level of assembly. For these reasons, the modular connectors shown in Fig. 3 were designed. The following subsections describe three main chassis designs which have been utilized in the DSN and for which documentation exists.

### A. Chassis With One or Two Subchassis

Figure 17 shows an assembly which holds one or two subchassis. The original design was developed by one of the DSN development engineers and has been adopted as a standardized assembly per drawing 9457952. This assembly is designed to pivot out of the drawer for service; Figs. 18 and 19 show the pivot assembly installed in a Star Switch Controller 9501300.

### B. Chassis With Multiple Subchassis

Figure 20 shows a chassis drawer assembled out of modular components. Figures 21 and 22 show the Metric Data Assembly assembled using these components. Two typical assemblies are documented in JPL sample drawing 9468707. These modular components were developed to meet the following requirements:

- (1) The drawer should be able to slide in and out of the cabinet while carrying several hundred system interface wires. The DSN standard interface cable design, with its stiff and heavy molded jacket, poses a severe problem if several of the larger cables must move in and out with the drawer slides.
- (2) The design should be capable of packaging up to six or seven subchassis, or a lesser number of other digital

devices or a self-contained power supply, using a maximum number of off-the-shelf mechanical components. Space should be available for front panel displays, if necessary.

The first objective was met by a design which does not attempt to draw the DSN standard cables in and out with the drawer slides; they mate with a rigidly mounted connector panel as shown in Fig. 23. Woven cables (preferably flat) provide connections to the chassis assembly. They track in and out with the drawer slides, excess cable lying in a tray. The chassis connections are made through a connector designed to mate with a wirewrap receptacle using the same contacts and wrap-post as the subchassis receptacle (Fig. 24). Thus, the connections among the subchassis and with the interface cables can all be made with wirewrap (see Fig. 22). The first user of this design reports that jumpers between the DSN standard interface cables should be made by carrying the wires up to chassis wirewrap level where the advantages of wirewrap changes are available.

The second objective was met with the modular design in which the user installs subchassis receptacles only where necessary. Deep panel displays may be accommodated by leaving the first receptacle position behind the front panel vacant (Fig. 20). As many cable receptacles may be installed (at the rear) as necessary, at the sacrifice of subchassis slots. Blank panels should be used to fill any unused space; these blanks may also be used for coaxial fittings.

### **C. Chassis With Multiple Interface Cables**

The chassis assembly shown in Fig. 25 was designed (in conjunction with M. Galitzen, cognizant engineer for the Timing and Frequency Assembly) to meet the need for an interface with up to sixteen 128-pin DSN cables. These cables form an exceptionally heavy and rigid mass. Access was necessary for in-system testing; however, the use of intermediary cables of the type shown in Fig. 22 was undesirable because of the large number of wires. A decision was made to mount the subchassis vertically as shown in the photograph. No slides are needed because the subchassis are accessible from the front. A hinged door closes on the assembly when access is not needed for service. The rack space required for vertical mounting of the subchassis was needed in any instance for the 16 large cable connectors and for cable routing.

### **D. Procurement of Chassis Hardware**

All chassis hardware, with the exception of the receptacle mounting accessories listed in Table 1, must be procured by the user. The Cognizant Sustaining Engineer for hi-rel packaging maintains cognizance over the drawing sets for the Pivot Assembly 9457952 (Fig. 17, not including mounting drawer)

and the Modular Drawer Assembly 9468707 (Fig. 20). While consulting assistance is available, the user is responsible for all other drawings.

### **E. Subchassis Extender**

Access to the ICs or the wirewrap connectors in packaging systems utilizing two or more subchassis requires the use of a subchassis extender, JPL part 9458186, shown in Fig. 26.

## **IX. Current Design Efforts and Future Plans**

### **A. Half-Size Subchassis**

JPL drawings have been completed for a half-size subchassis (2 sections of the normal 4-section layout), and a model has been fabricated by cutting down a full-size subchassis. This half-sized subchassis will be included in our next subchassis procurement. The eventual quantity price is estimated at 65 percent of the full-size subchassis. The principal applications are expected to be found in subsystems which require only small numbers of microelectronic packages for which the cost or space savings are significant.

### **B. Accommodating LSI Components**

Additional consideration is now being given to the use of large-scale integration (LSI) microcontroller-processor packages which have up to 40 pins (future packages may have up to 80 pins) arranged in two rows with 0.6-in. (1.5-cm) spacing between rows (present 14 and 16 pin packages use 0.3-in. (7.6-mm) spacing).

These larger packages can be accommodated by removing some of the ground posts (ground posts are visible in the z-rows; i.e., 1z, 2z, 3z, etc., of Fig. 12) and installing additional socket strips in these z-rows, as shown in Fig. 27. This procedure sometimes requires the removal of existing sockets and the installation of new ground posts, in order to keep ground lead lengths short. R. Winkelstein has suggested a design modification which would eliminate the need for extensive customizing by providing ground posts alternating with the power posts in the x-rows, as illustrated in Fig. 28. This modification can be implemented at modest expense. However, the DSN's continuing requirements for the existing model (if only to build additional copies of existing subsystems) would result in the stocking of two different subchassis versions. This arrangement would not be too painful, since subchassis could be converted from one version to the other simply by moving the ground posts. A decision has been made to make mechanical provisions for the new ground post location in the next units to be manufactured, but to install all

ground posts in the current z-row locations. However, the half-size subchassis will be provided with ground posts installed in the new location.

### **C. Development of Inspection Aids**

Training inspectors to perform source inspection of subchassis has been difficult because of a lack of training aids. It has been recognized that photographs of manufacturing defects would be useful, and 15 photographs were taken during the last contract. Additional photographs should be taken during the next contract and descriptive material added. No decision has been made whether to publish these photo-

graphs in a formal document or simply to retain sets in the offices of the cognizant sustaining engineer and the QA Supervisor.

### **D. Other Mounting Techniques**

Most chassis designs require the use of an extender if access is required to subchassis ICs or wirewrap during in-system testing. Some thought has been given to the possibility of a design similar to that of the standard minicomputer currently used in the DSN; wirewrap boards in these minicomputers fold out as the pages in a book. No plans for a full-scale development project have been formulated to date.

## **Reference**

1. Slaughter D.W., "Hi-Rel Integrated Circuit Packaging Development," in *The Deep Space Network*, Technical Report 32-1526, Vol. VII, pp. 113-123, Jet Propulsion Laboratory, Pasadena, Calif., Feb. 15, 1972.

**Table 1. Parts list of hi-rel standard packaging hardware**

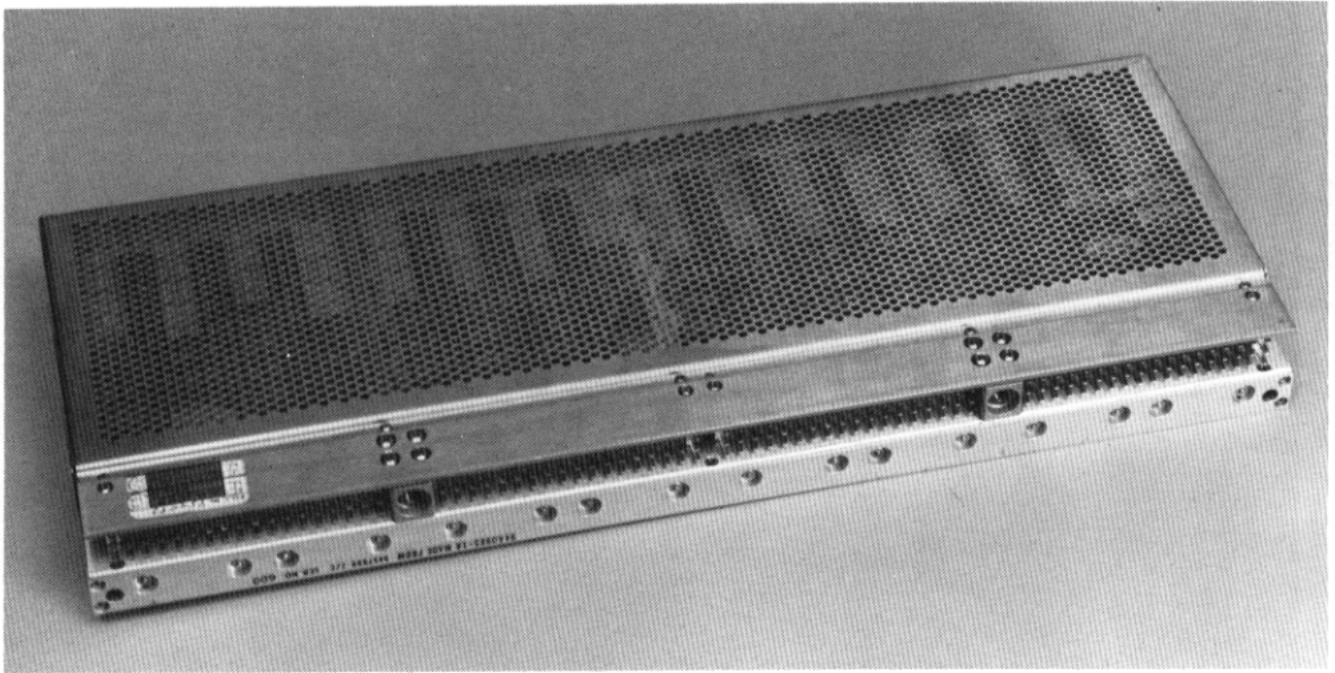
Part description	Note	Part No.	Reference figure	Cost,* \$
Subchassis (full-size)	1	9457999**	1	800.00
Subchassis (half-size)		9458904-1		520.00
Receptacle, wirewrap		9459013-1	3	56.00
Receptacle, wire-crimp		9459014-1	3	60.00
Ground bus	2	9458877-1	3	3.00
Stiffening rail, ventilating	3	9459033-1	3	6.00
Stiffening rail, nonventilating	4	9460106-1	3	6.00
Ball catch	5	9501223-1	17	free
Subchassis extender		9458186**	26	480.00
IC modular socket	6	9457910-1	6	0.50
Wrap-post, ground	6	9457084-1	—	0.25

\*Prices may vary depending on quantities (combined JPL requirements) ordered and the state of the commercial market.

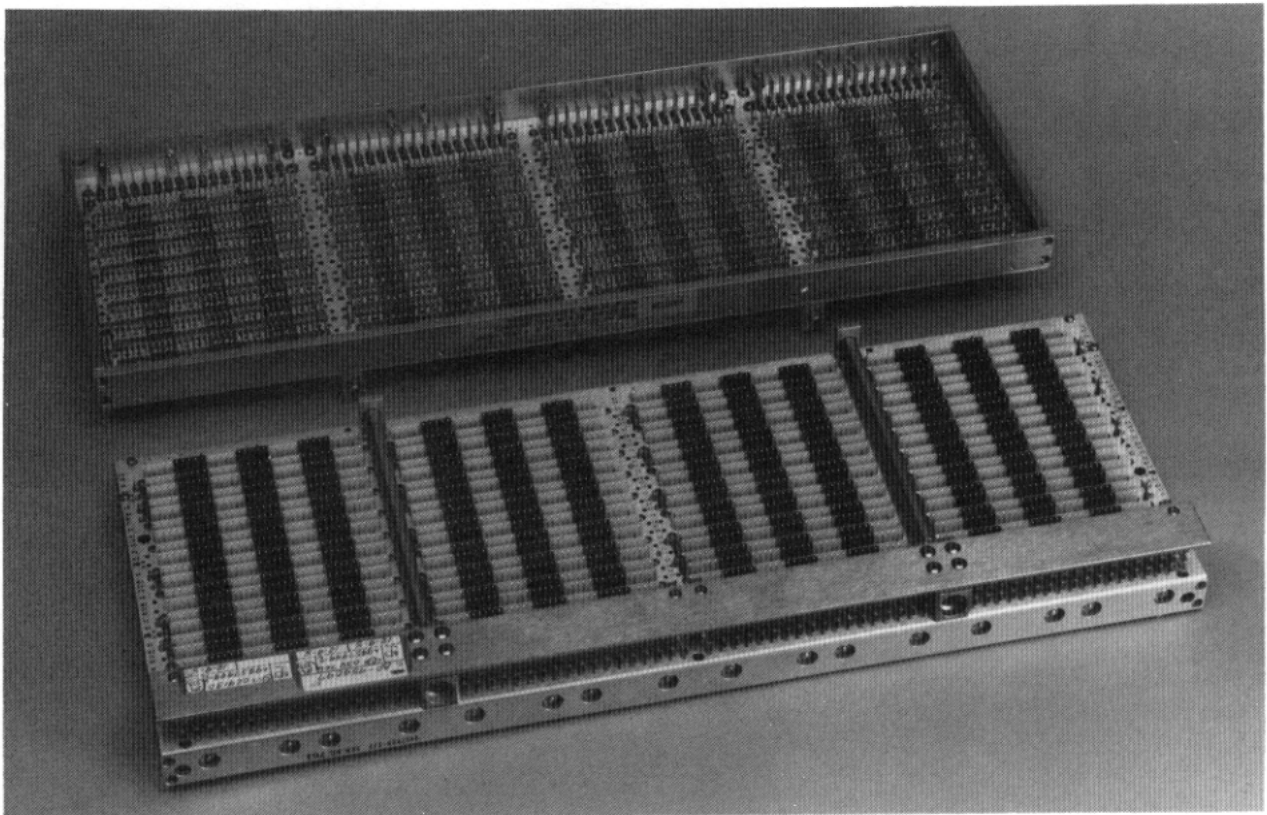
\*\*May be supplied as -1 or -2 versions. Dash numbers cover manufacturing differences only; parts are interchangeable to the user who should list part with both dash numbers, for example 9457999-1 or -2.

#### NOTES

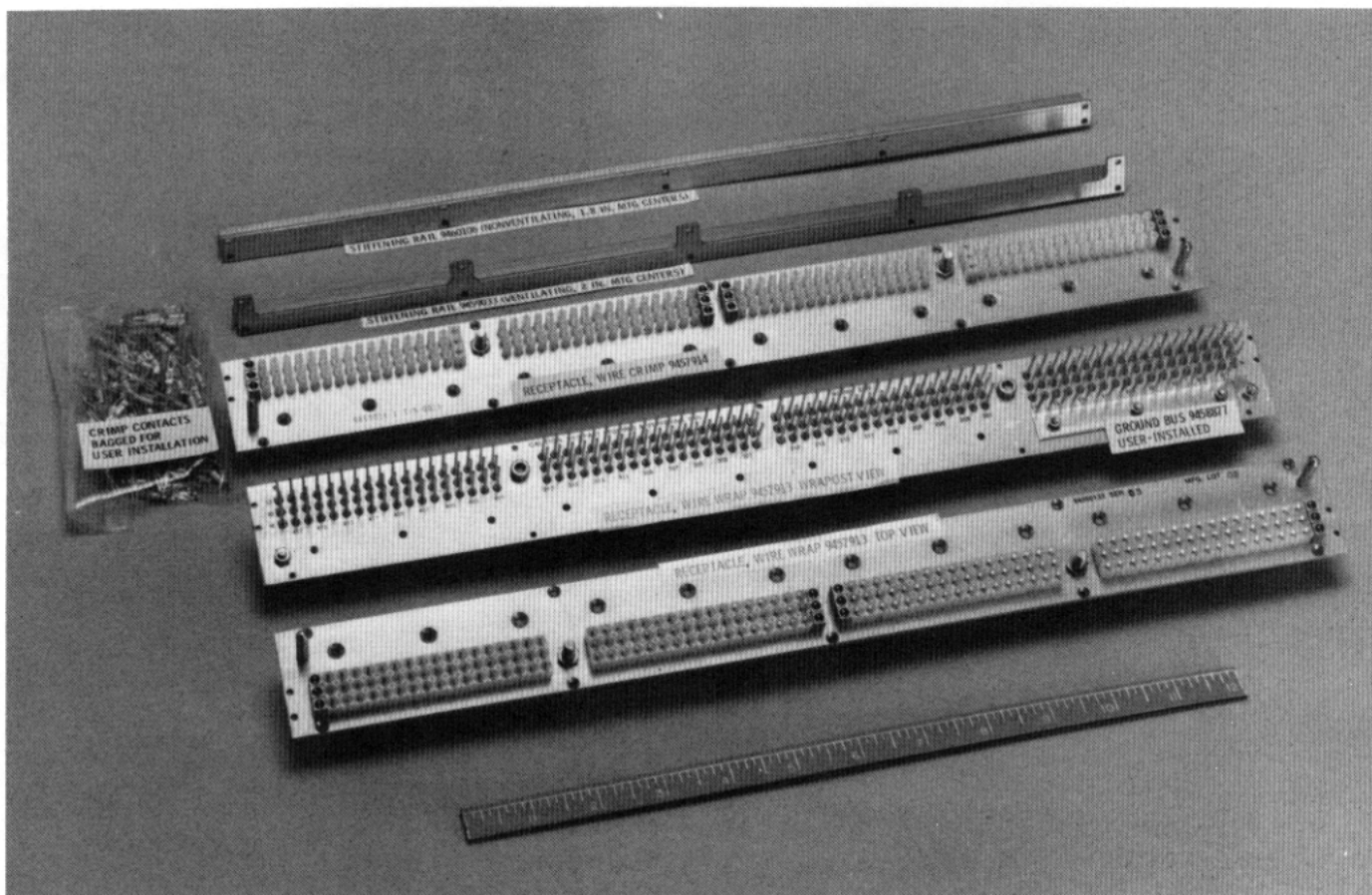
1. Future procurement only; not in stock.
2. Mounts on receptacle; use to ground shields or twisted pairs.
3. Mounts receptacles on 2-in. (5.08-cm) centers and allows for air flow between receptacles.
4. Mounts receptacles on 1.8-in. (4.57-cm) centers.
5. Used on pivot assembly 9457952.
6. Install on subchassis as required to accommodate LSI packages.



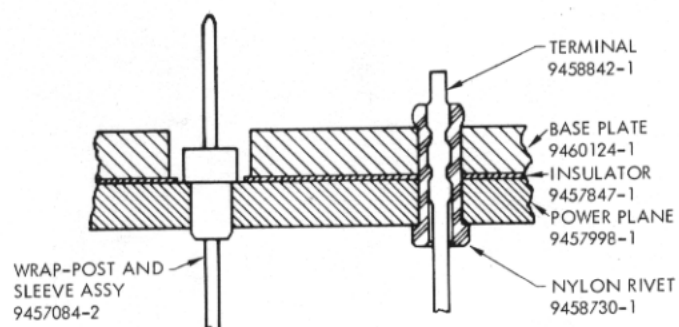
**Fig. 1. Subchassis with cover installed**



**Fig. 2. Socket and wirewrap sides of subchassis**



**Fig. 3. Receptacles and stiffening rails**



**Fig. 4. Power plane with power pin and rivet**

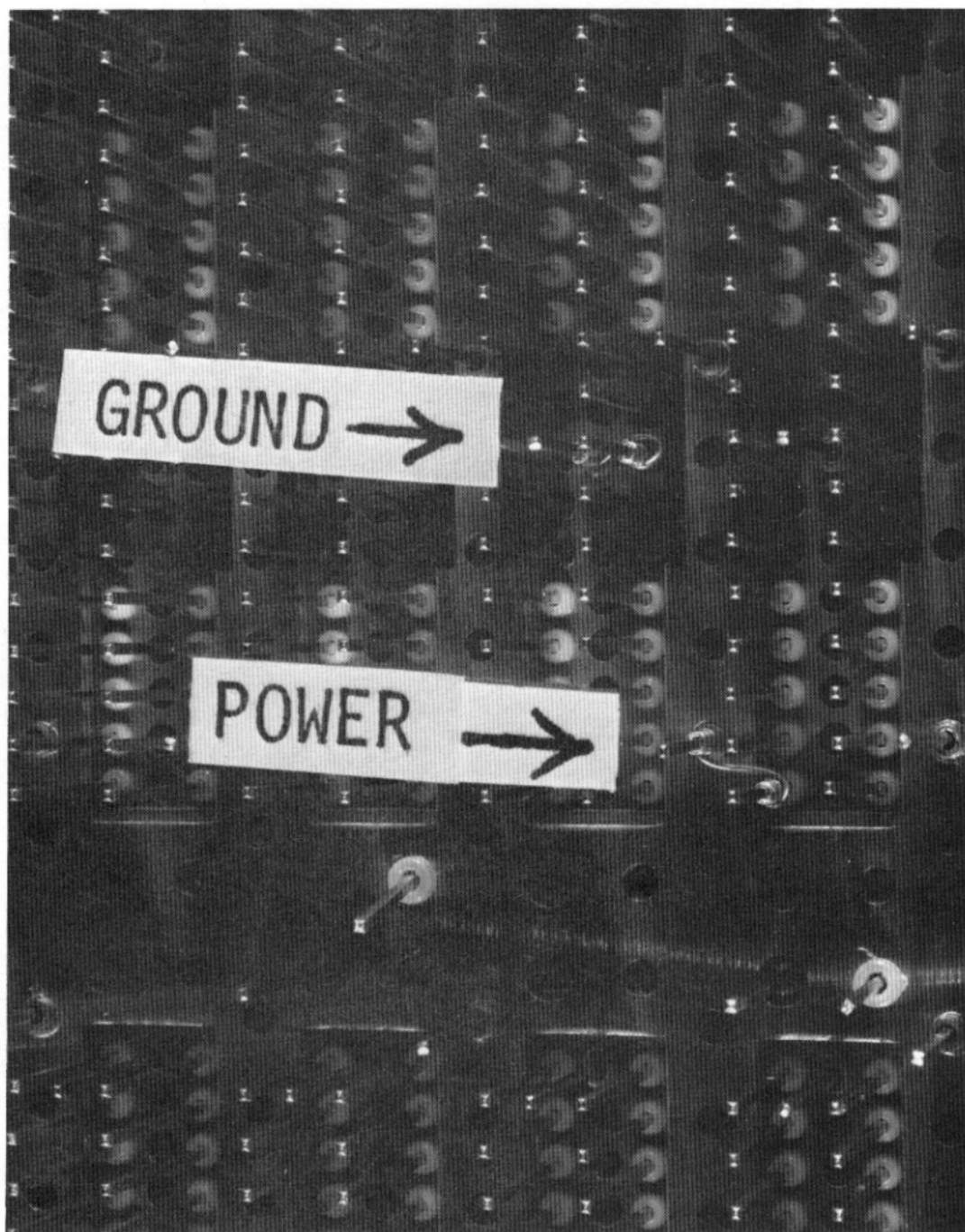


Fig. 5. Wirewrapped ground and power connections

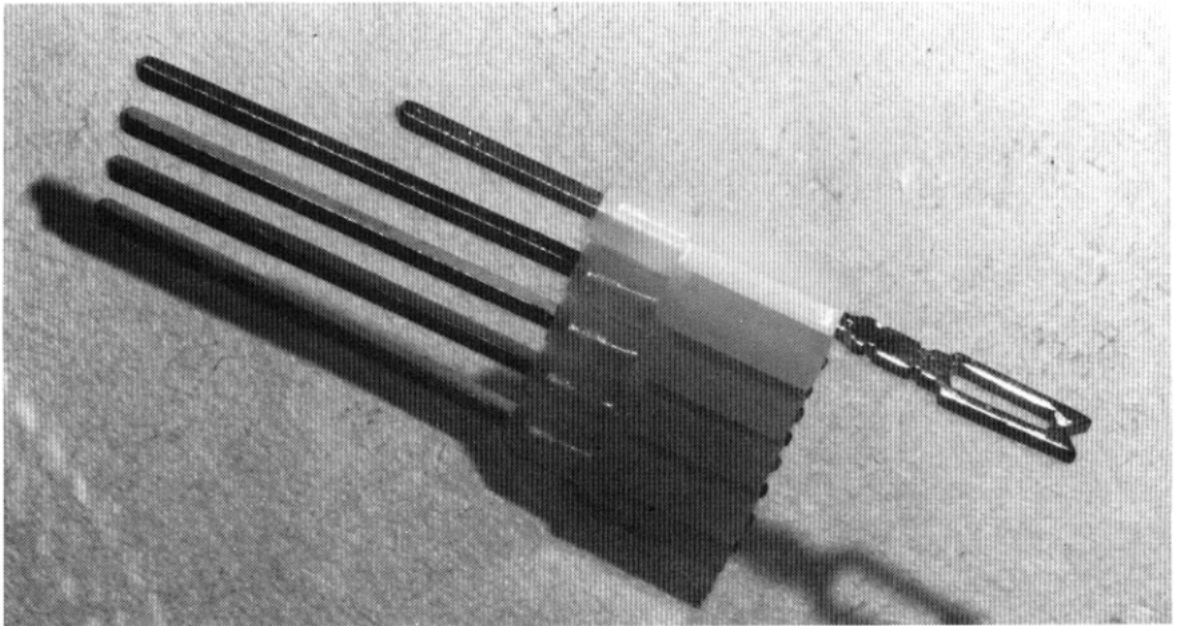


Fig. 6. IC strip socket

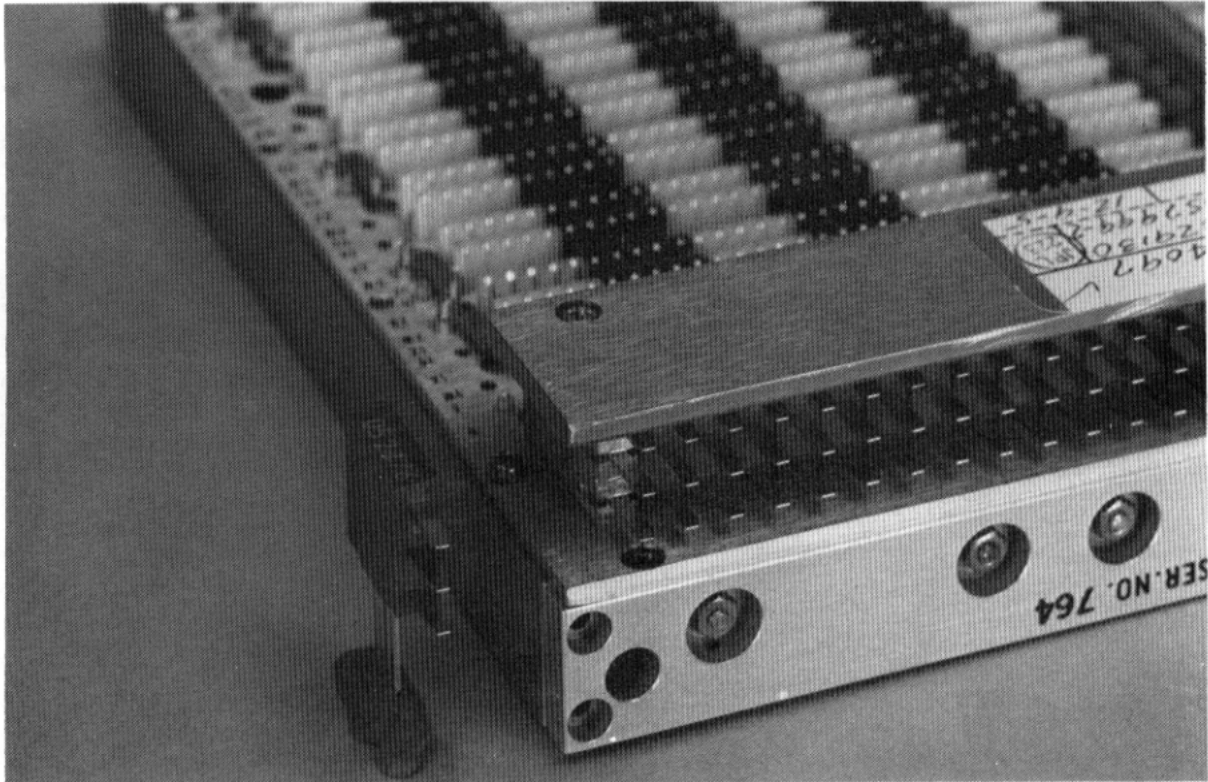
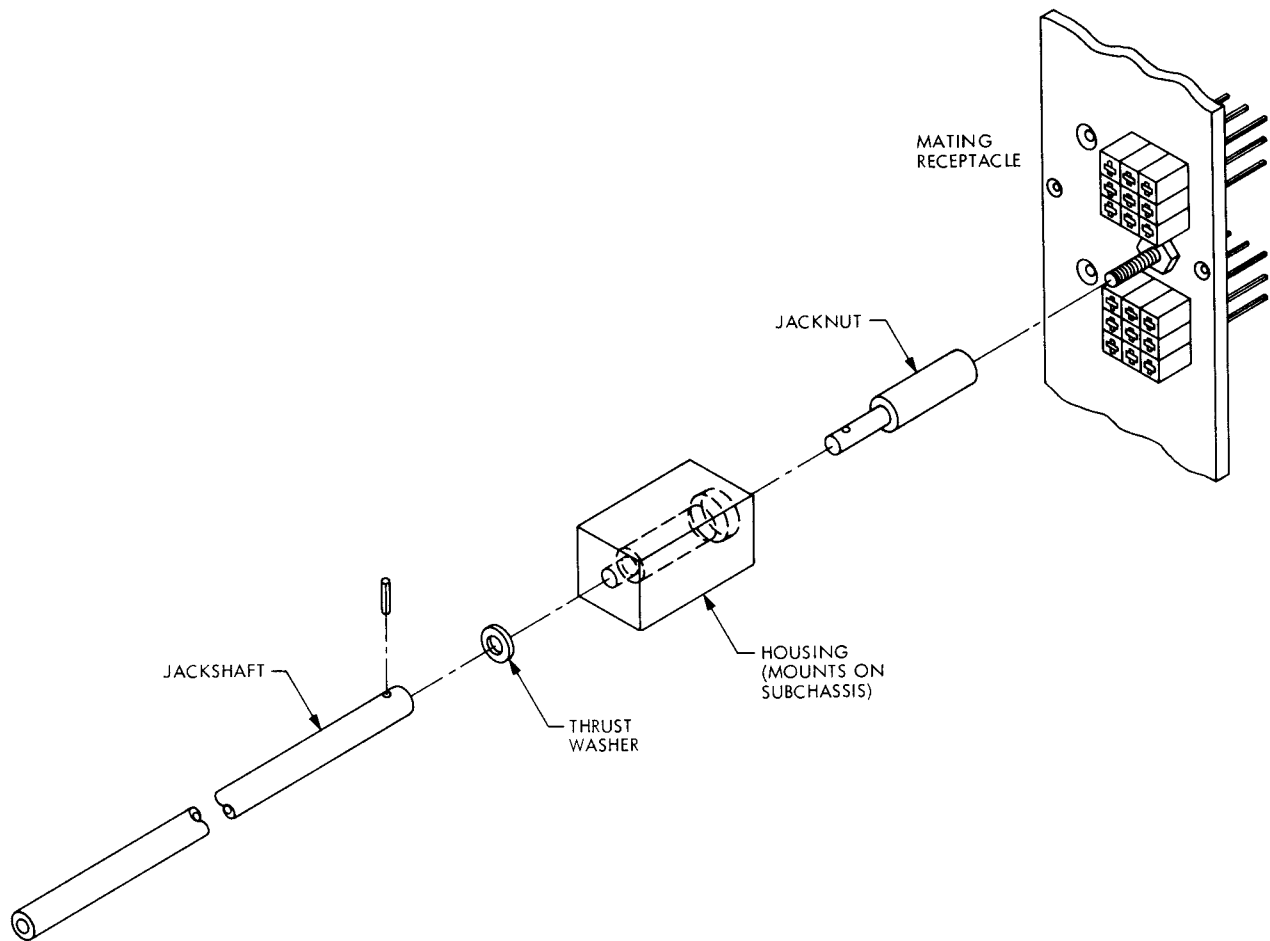
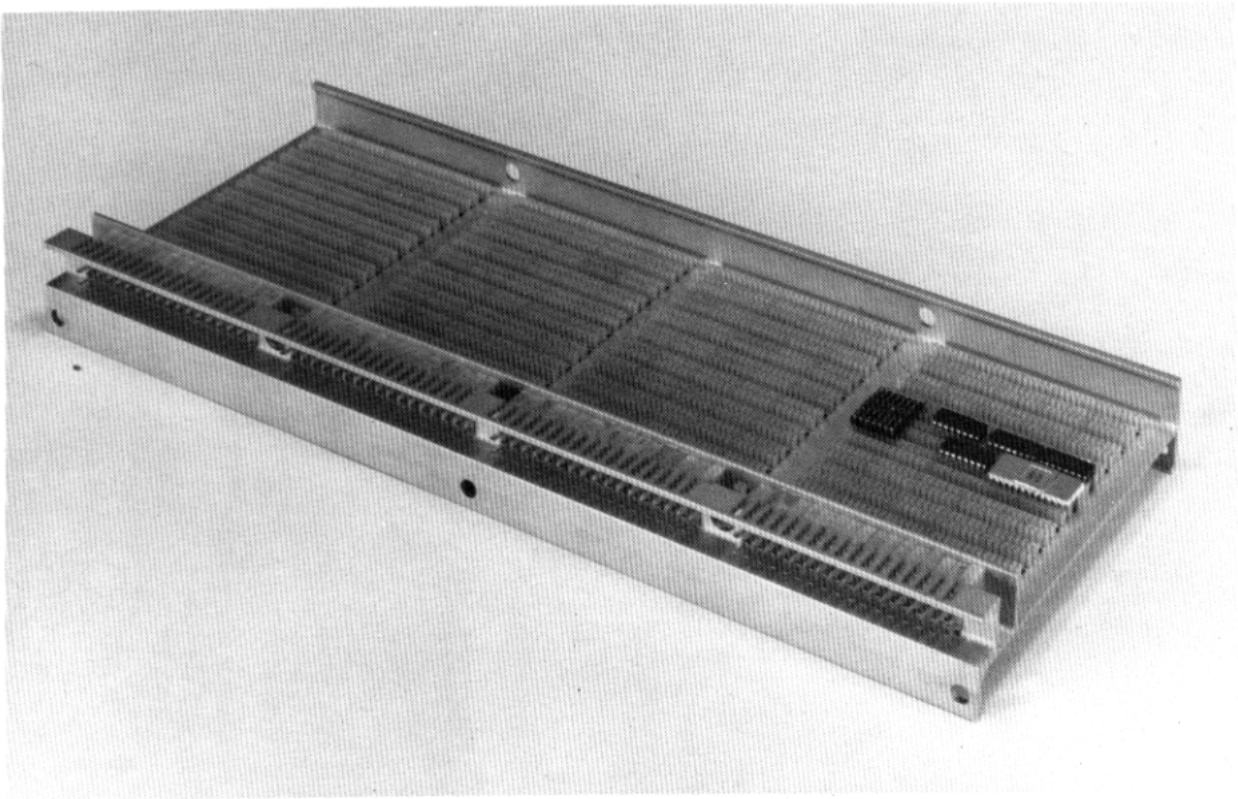


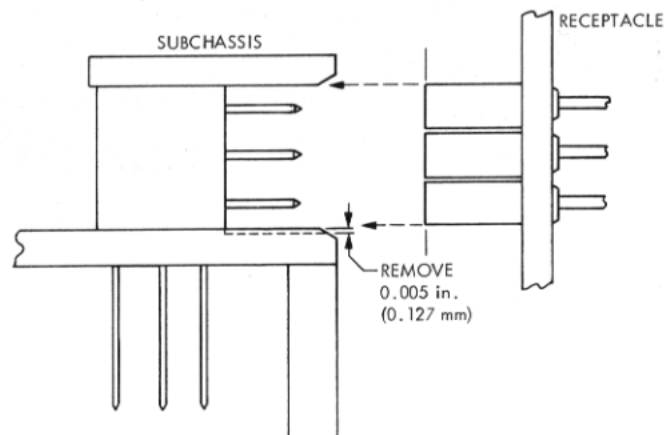
Fig. 7. Modular connector



**Fig. 8. Jackscrew assembly**



**Fig. 9. Obsolete design of extruded subchassis**



**Fig. 10. Subchassis to receptacle mating**

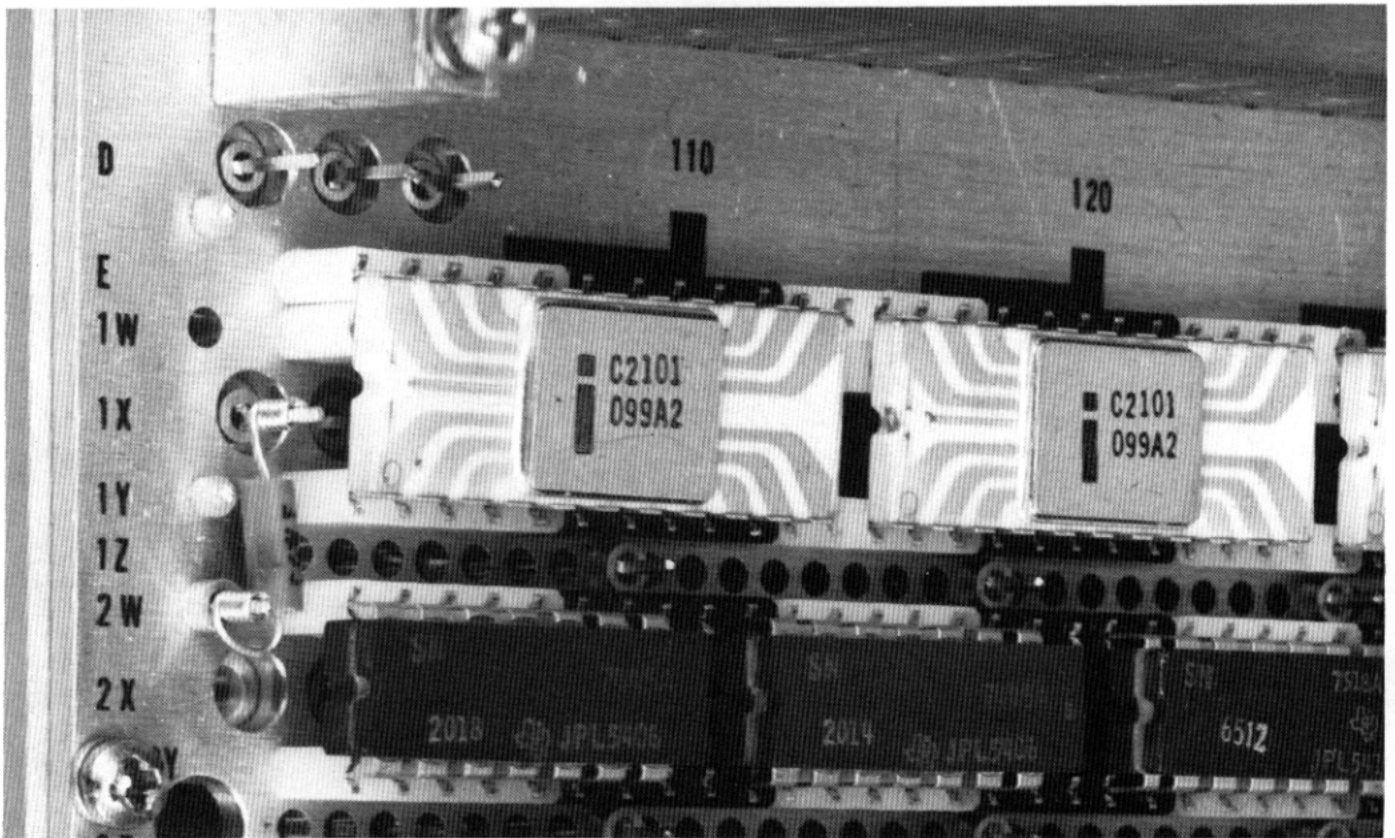


Fig. 11. LSI microcircuits mounted in user-installed strip sockets

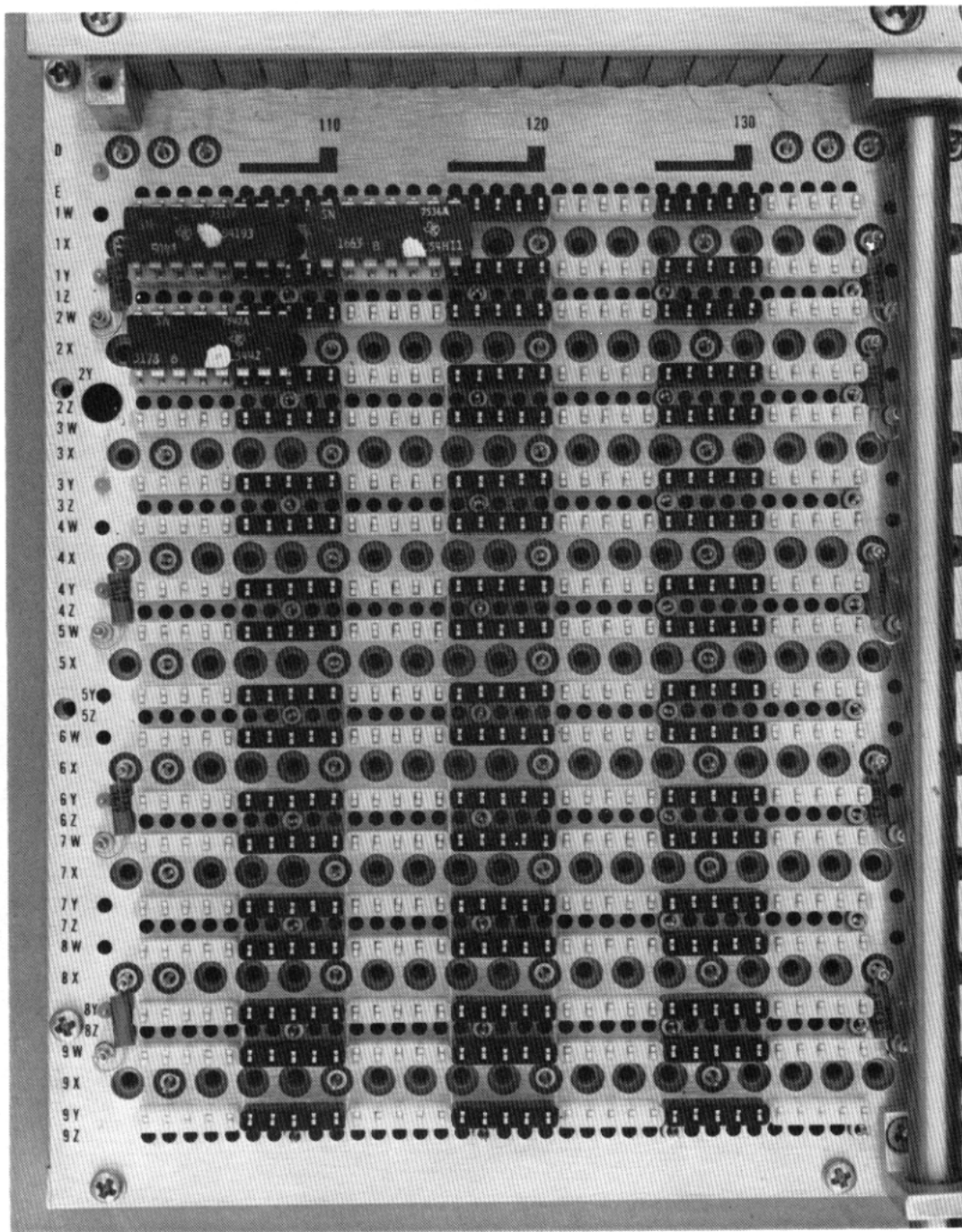
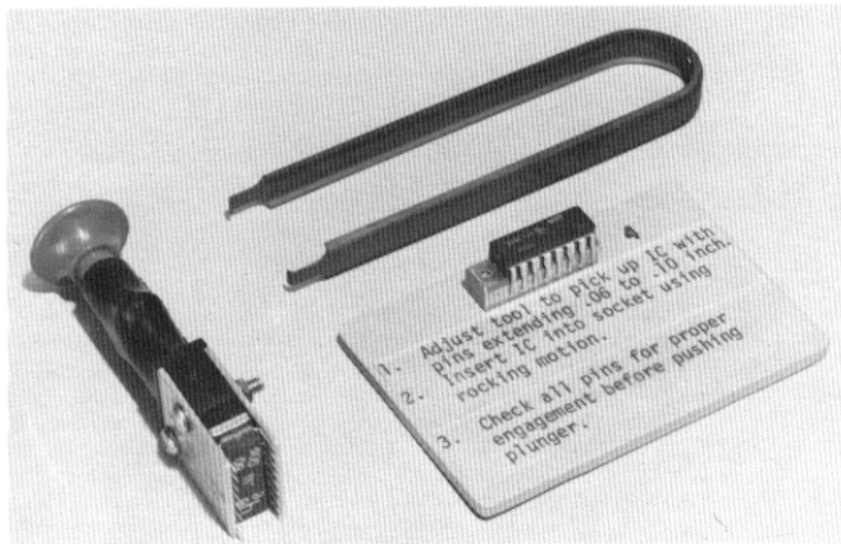


Fig. 12. One section of subchassis showing numbering system



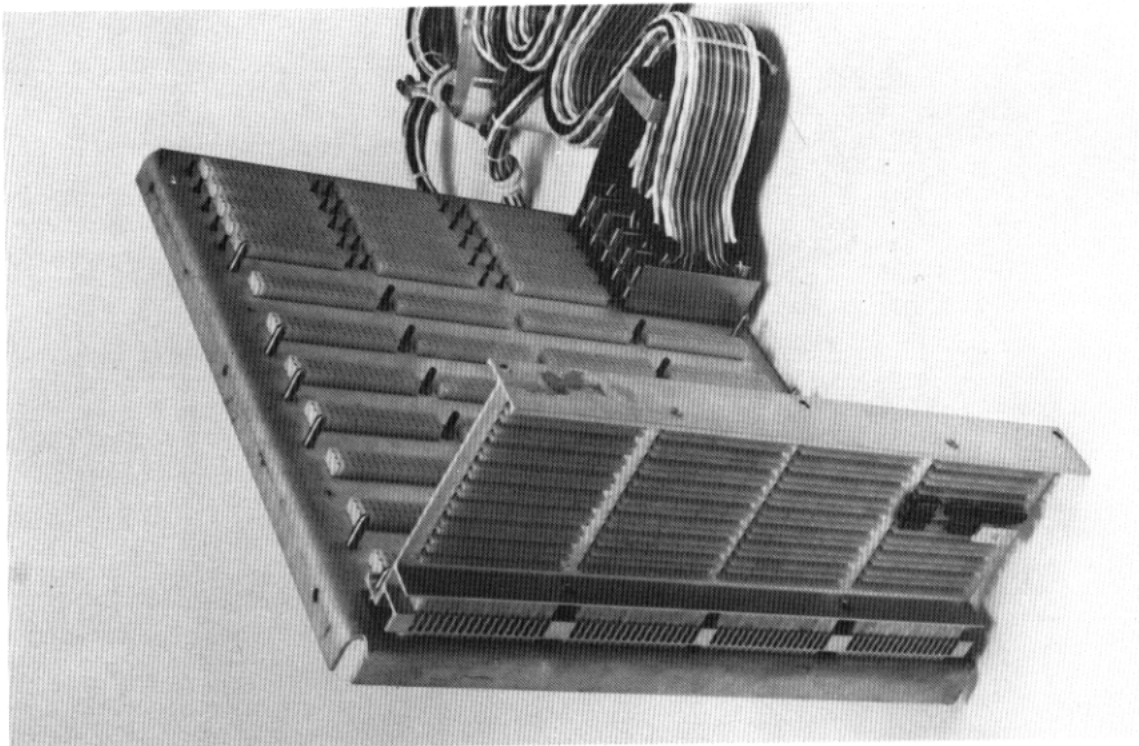
**Fig. 13. IC insertion and removal aids**



**Fig. 14. Subchassis maintenance tool kit**



**Fig. 15. Wirewrap receptacle maintenance tool kit**



**Fig. 16. Custom design of main chassis**

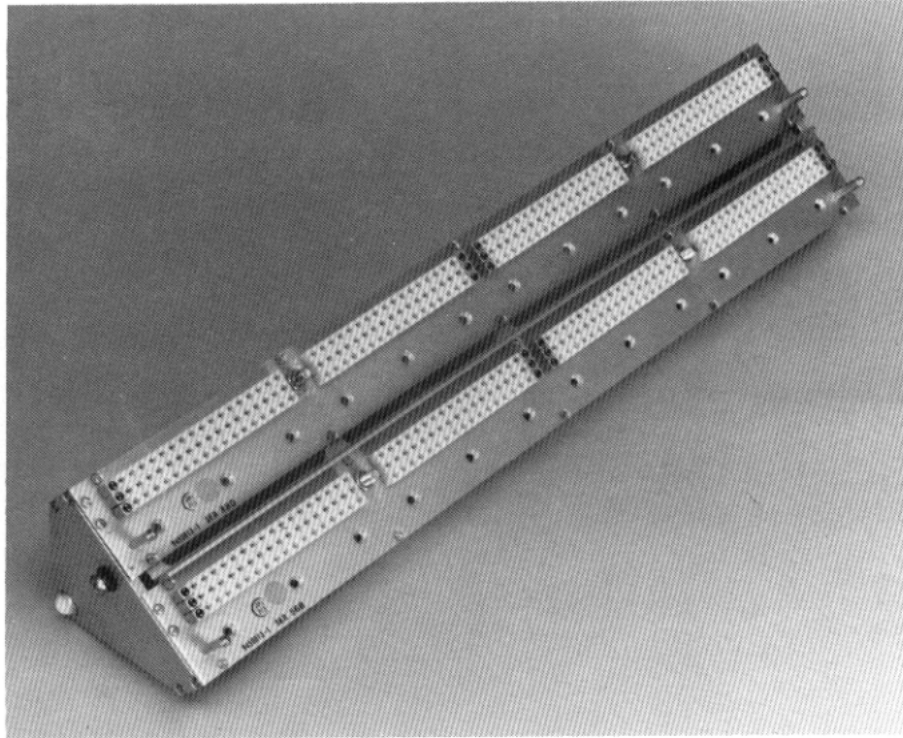


Fig. 17. Pivoting receptacle assembly

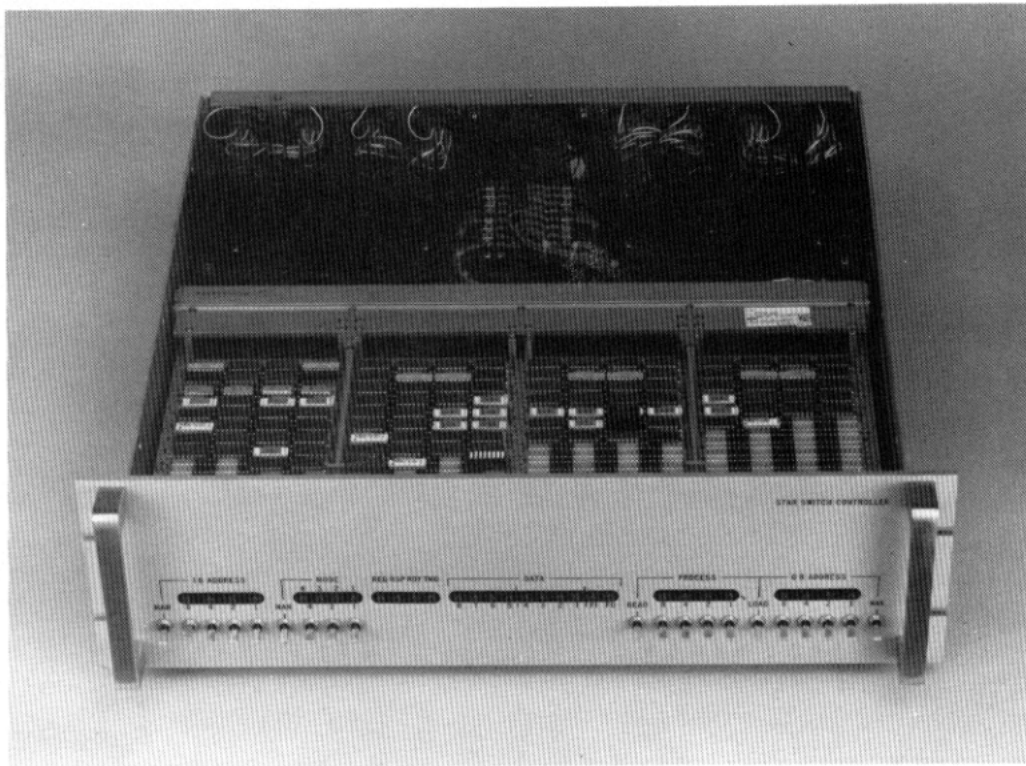


Fig. 18. Star switch controller

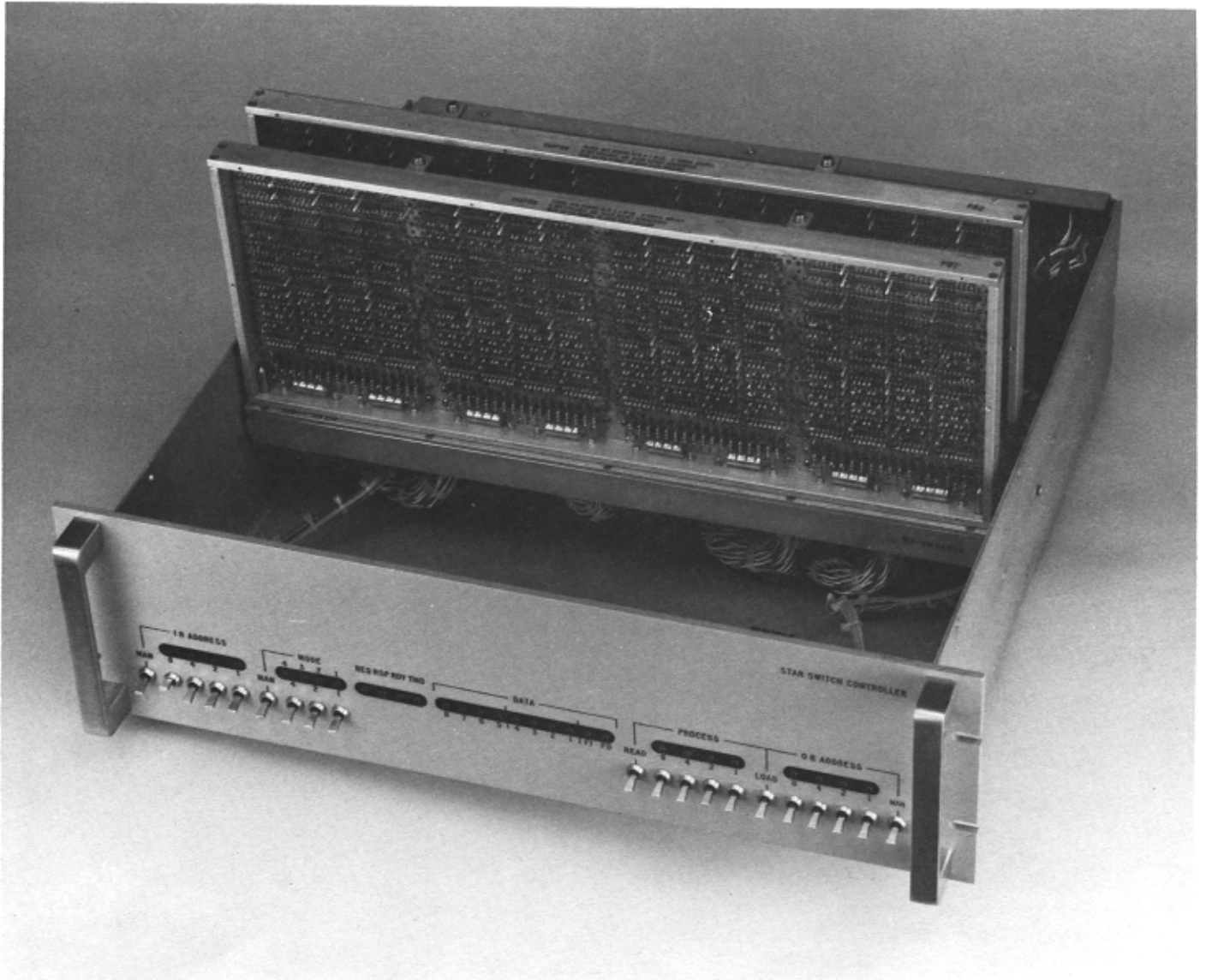
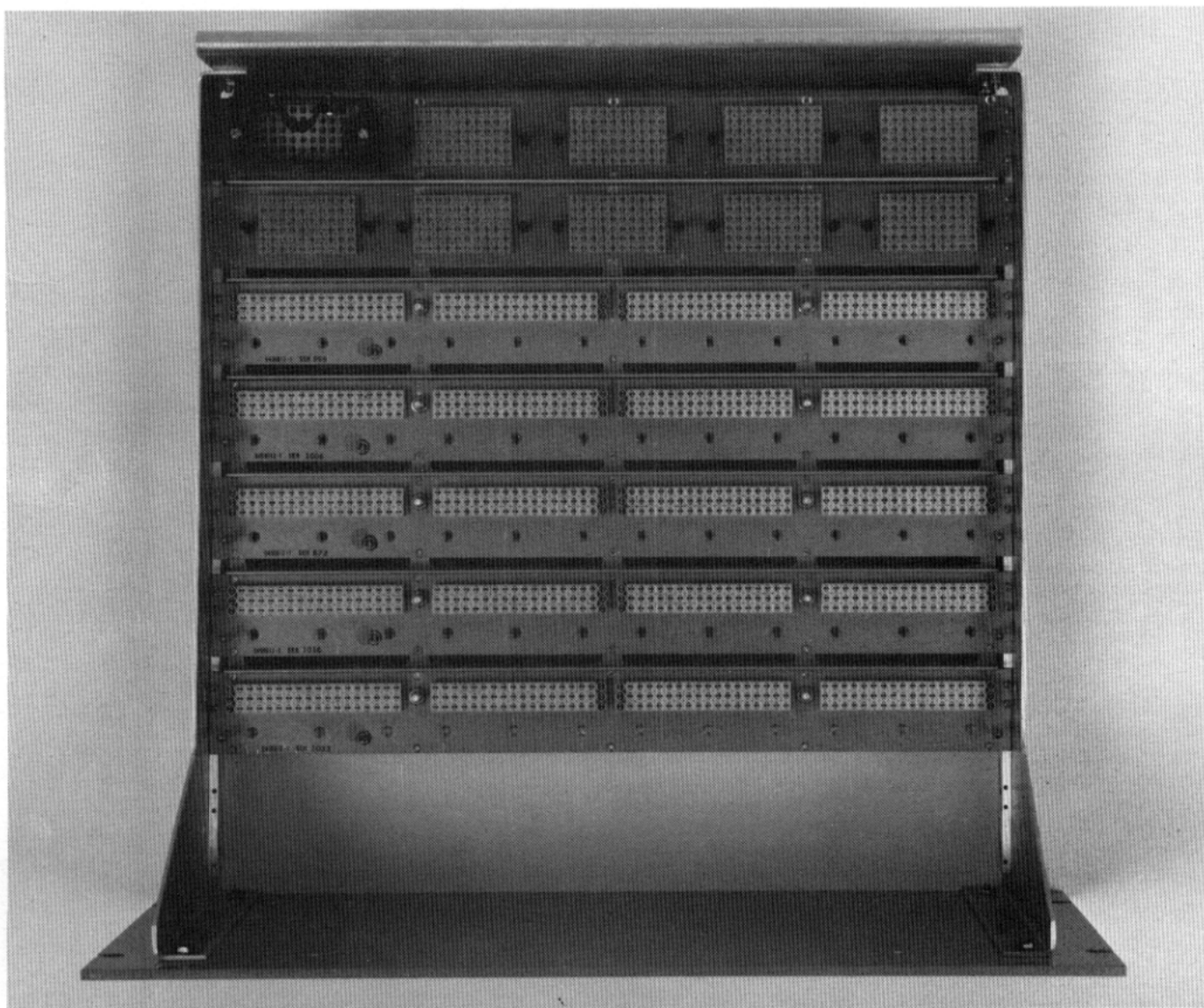
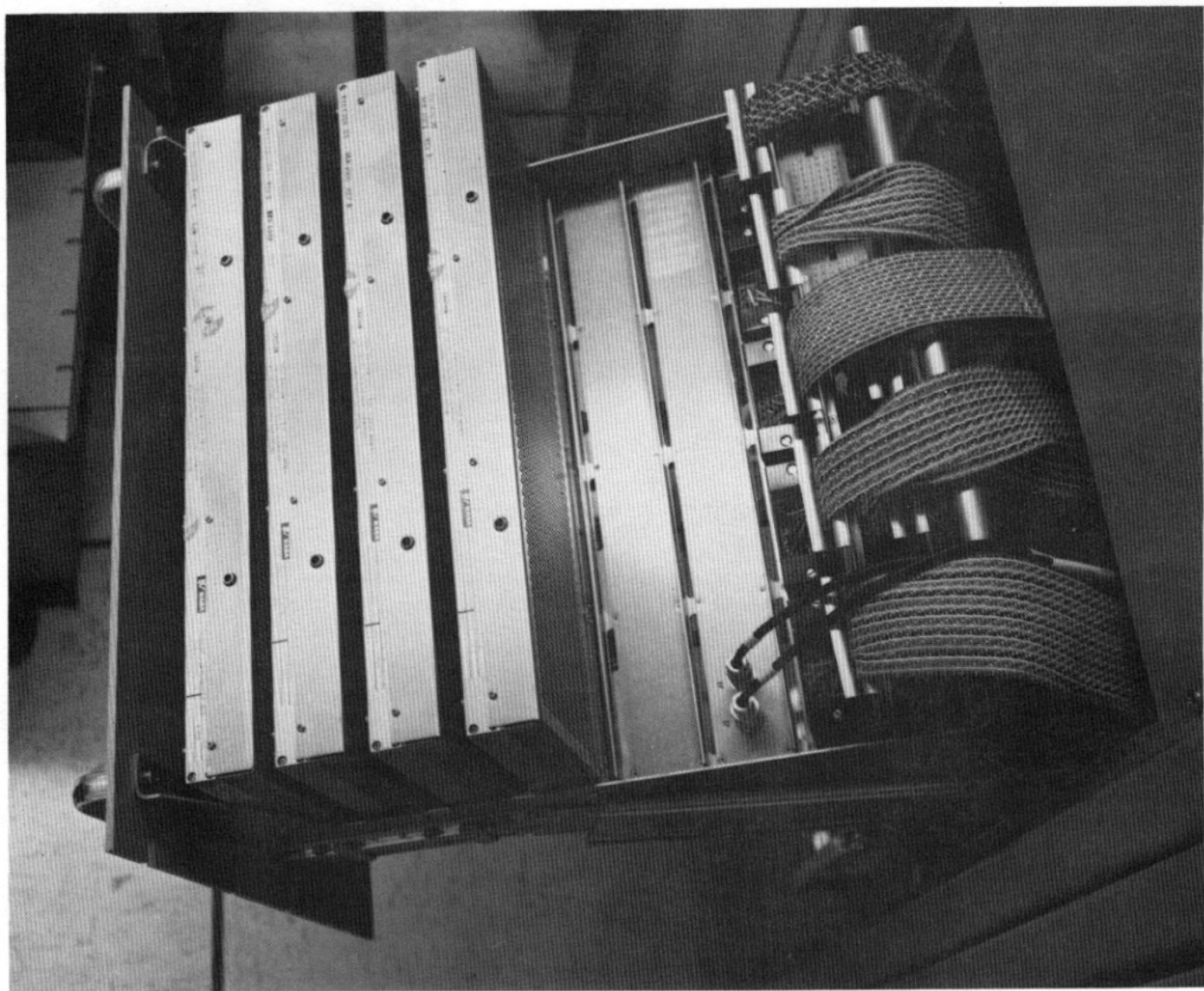


Fig. 19. Star switch in service position



**Fig. 20. Modular Drawer Assembly with one receptacle omitted to provide space for panel-mounted indicators**



**Fig. 21. Metric Data Assembly packaged with modular components**

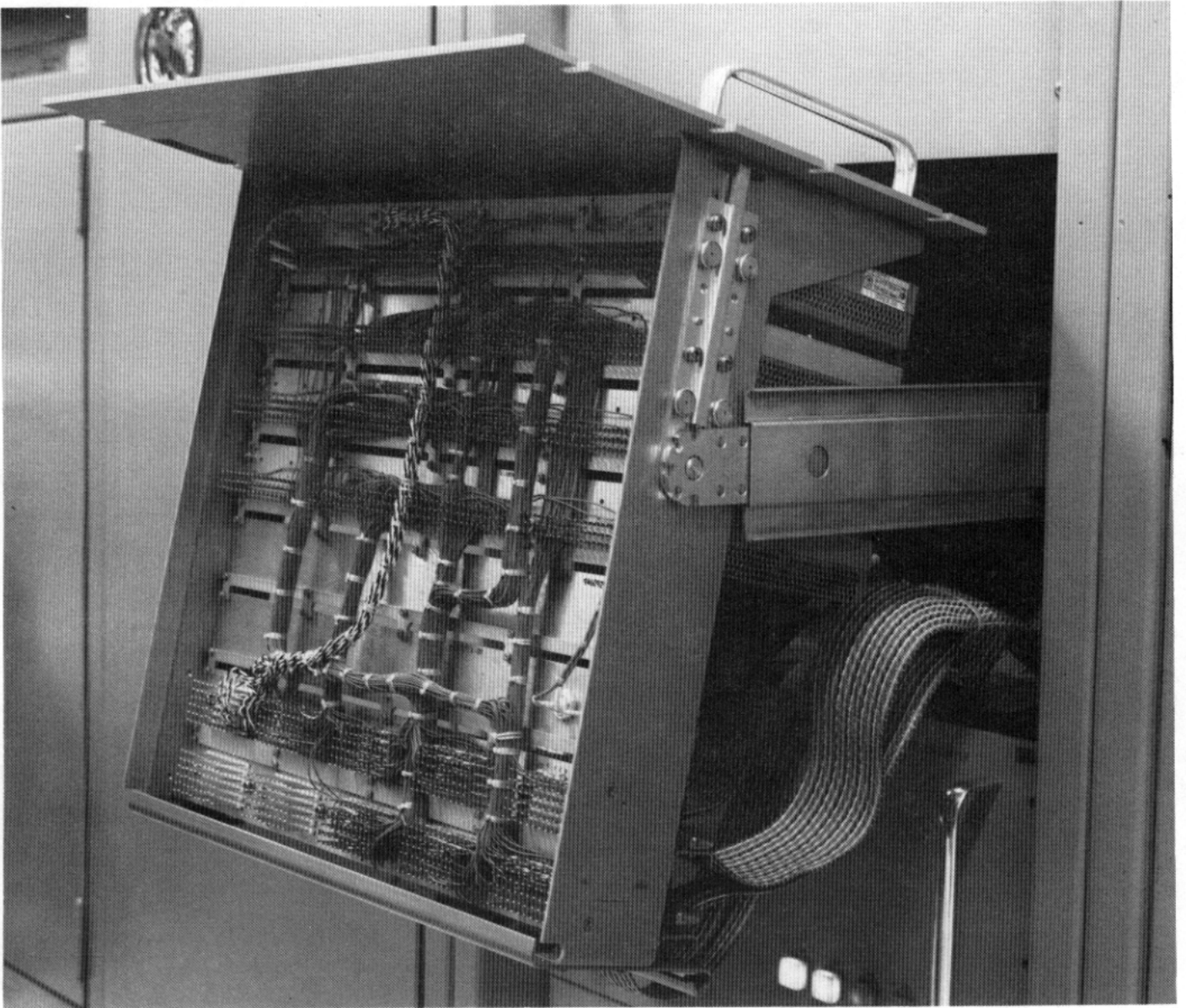
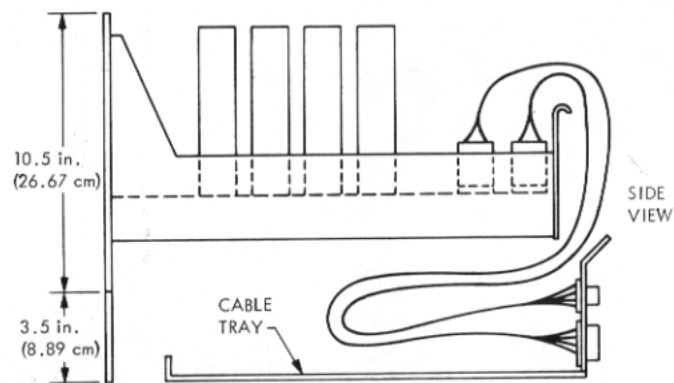
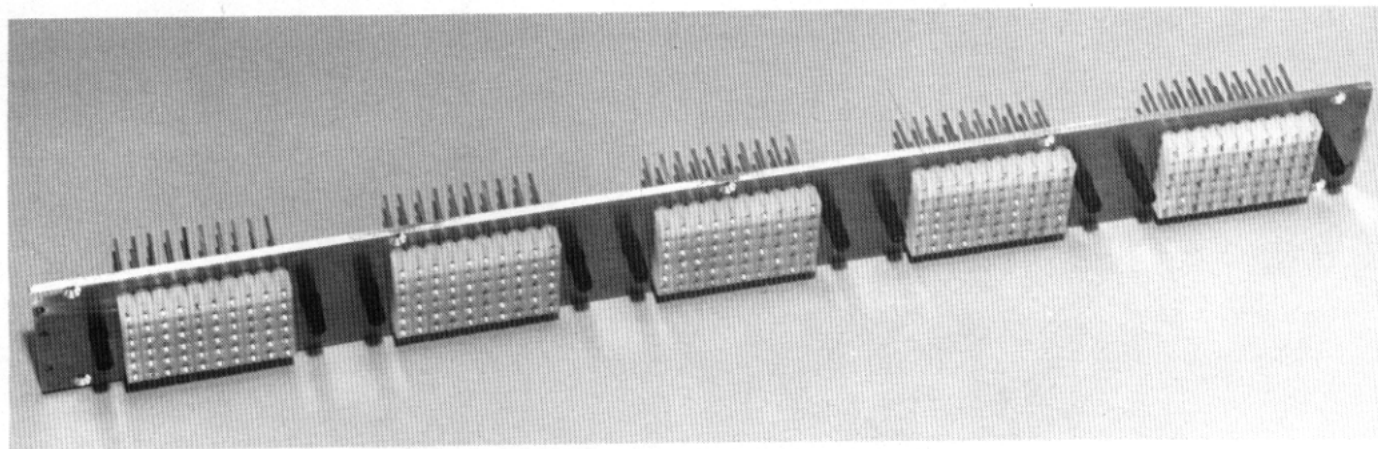


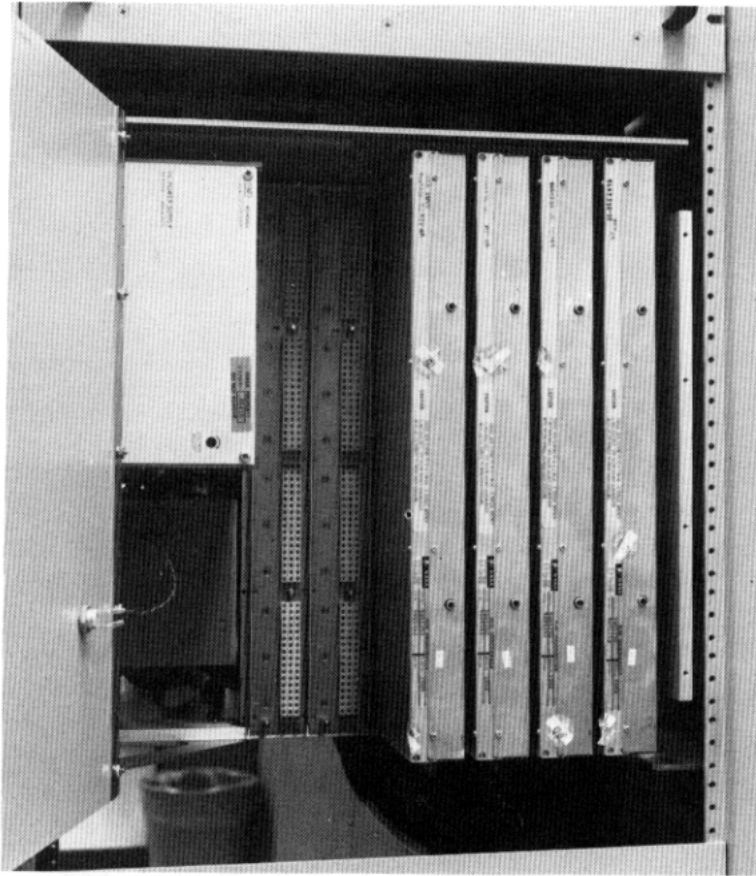
Fig. 22. Metric Data Assembly



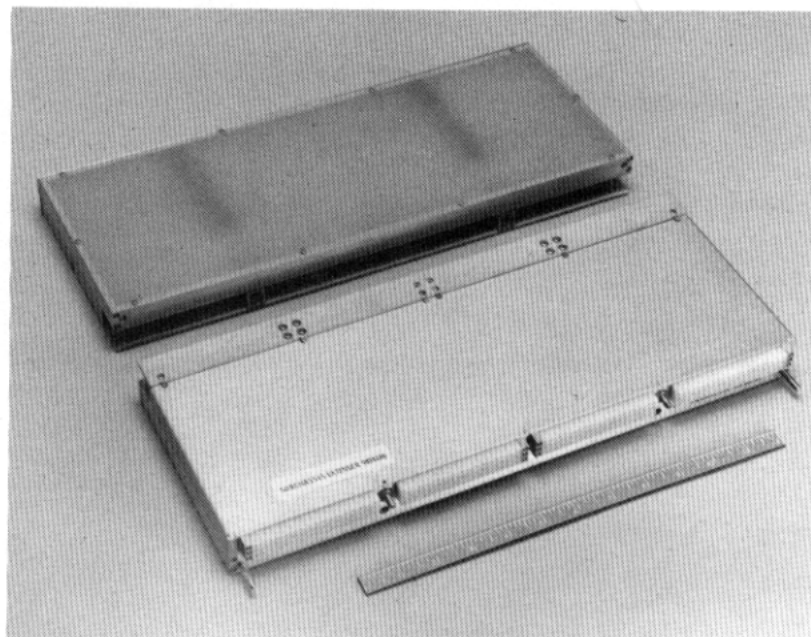
**Fig. 23. Modular drawer with cable tray**



**Fig. 24. Cable receptacle showing receptacle used in Modular Drawer Assembly of Fig. 20**



**Fig. 25. Timing and Frequency Assembly**



**Fig. 26. Subchassis extender**

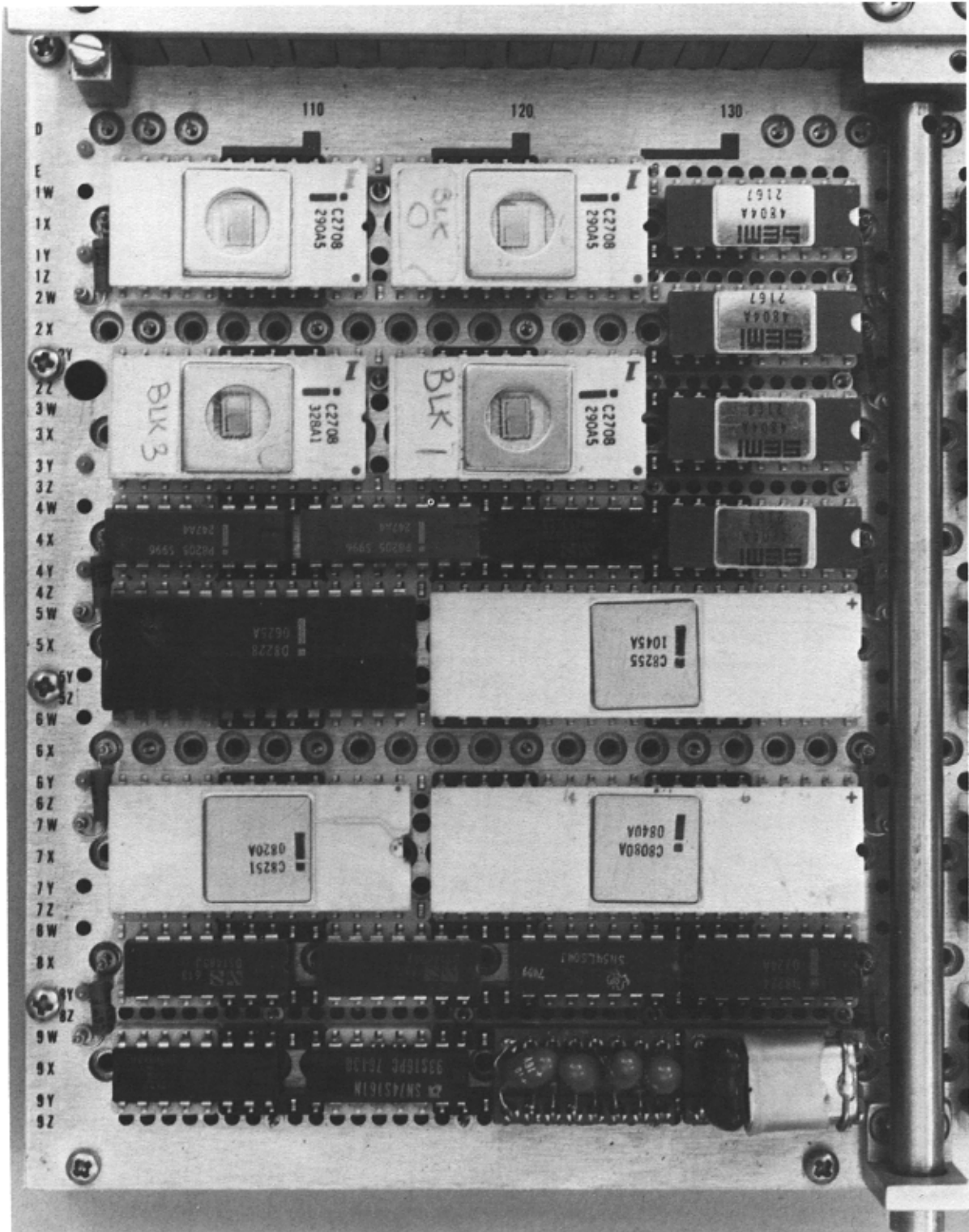


Fig. 27. Subchassis modified for microprocessor application

